## WHAT IS CLAIMED IS:

1	. A radio receiver, comprising:
2	an amplifier configured to receive and amplify an intermediate frequency
3	modulated signal having in-phase and quadrature phase DC components;
4	an analog-to-digital converter configured to receive the amplified intermediate
5	frequency modulated signal and convert it to a digital signal;
6	a demodulator operable to demodulate the digital signal; and
7	DC offset calibration means coupled to the demodulator operable to provide
8	in-phase and quadrature phase DC offset correction signals to compensate for the in-phase
_9	and quadrature phase DC components at the input of the amplifier.
1 11	2. The radio receiver of claim 1, further comprising:
_2	delay measurement means coupled to the demodulator operable to determine a
	delay vector characterizing the in-phase and quadrature phase DC components.
= 1	3. The radio receiver of claim 2, wherein the delay vector is used by the
2	DC offset calibration means to provide a digital representation of the in-phase and quadrature
113	phase DC offset correction signals.
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-	4. The radio receiver of claim 3, further comprising:
2	a first digital-to-analog converter configured to receive a in-phase component
3	of the digital representation of the in-phase DC offset correction signal for mixing with an in-
4	phase signal and an intermediate frequency carrier signal;
5	a second digital-to-analog converter configured to receive a quadrature phase
6	component of the digital representation of the quadrature phase DC offset correction signal
7	for mixing with a quadrature signal and the intermediate frequency carrier signal; and
8	a summer operable to subtract the mixed quadrature phase signal and
9	quadrature phase DC offset correction signal component from the mixed in-phase signal and
10	in-phase DC offset correction signal to provide a DC compensated intermediate frequency
11	modulated signal at the input of the low noise amplifier.
1	5. A radio receiver, comprising:
2	a receiving stage configured to receive a radio signal;
3	a first mixer stage operable to downconvert the radio frequency signal to a
4	first intermediate frequency in-phase signal and a first intermediate quadrature phase signal;

5	first and second low pass filters configured to receive and low pass filter the
6	first intermediate frequency in-phase and quadrature phase signals;
7	a second mixer stage operable to upconvert the filtered first intermediate
8	frequency in-phase and quadrature phase signals and provide a second intermediate
9	frequency in-phase signal and a second intermediate frequency quadrature phase signal;
10	a summer operable to subtract the second intermediate frequency quadrature
11	phase signal from the second intermediate frequency in-phase signal to provide an integrated
12	signal;
13	an automatic gain control stage coupled to the summer and operable to
14	amplify the integrated signal;
15	an analog-to-digital converter operable to convert the amplified integrated
16	signal to a digital signal;
	a demodulator operable to demodulate the digital signal; and
18	delay measurement means for determining a delay vector from inputs of the
19	low pass filters to an output of the demodulator.
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	6. The radio receiver of claim 5, further comprising:
	a DC offset calibrator coupled to the delay measurement means;
ر 4	an in-phase digital-to-analog converter coupled between the DC offset calibrator and the second mixer stage; and
5	•
6	a quadrature phase digital-to-analog converter coupled between the DC offset calibrator and the second mixer stage,
7	wherein the in-phase digital-to-analog converter is operable to provide an in-
8	phase DC offset compensation signal for the automatic gain control stage and the quadrature
9	phase digital-to-analog converter is operable to provide a quadrature phase DC offset
10	compensation signal for the automatic gain control stage
10	compensation signal for the automatic gain control stage
1	7. A method of determining a signal delay between inputs of first and
2	second low pass filters of a dual mixer stage radio receiver and an output of the receiver's
3	demodulator, the method comprising the steps of:
4	applying a first known voltage to an input of an in-phase mixer of the second
5	mixer stage;
6	applying a second known voltage to an input of a quadrature phase mixer of
7	the second miver stage:

δ	setting the gain of an automatic gain control stage, coupled to the second
9	mixer stage, to a full gain; measuring first in-phase and first quadrature phase components at
10	the output of the demodulator;
11	decreasing the gain of the automatic gain control stage by a predetermined
12	amount if the value of each first component is greater than a predetermined maximum
13	threshold value;
14	storing the first in-phase and quadrature phase components if the value of each
15	component is less than the predetermined maximum threshold value;
16	applying the negative of the first known voltage to the input of the in-phase
17	mixer;
18 19 20 21 22	applying the value of the second known voltage to the input of the quadrature phase mixer;
$\overline{2}0$	measuring second in-phase and second quadrature phase components at the
<b>2</b> 1	output of the demodulator;
<b>2</b> 2	decreasing the gain of the automatic gain control stage by a predetermined
23	amount if the value of each second component is greater than the predetermined maximum
24	threshold value;
24 25 26	storing the second in-phase and quadrature phase components if the value of
26	each second component is less than the predetermined maximum threshold value; and
27	using the first and second quadrature phase components to compute the signal
28	delay
1	8. A method of compensating for DC offset voltages present at an input
2	of a low noise amplifier of a dual mixer stage radio receiver, the method comprising the steps
3	of:
4	determining a signal delay between an output of a second mixer stage of the
5	dual mixer stage radio receiver, said signal delay characterizing in-phase and quadrature
6	phase components of the DC offset voltage present at the input of the low noise amplifier;
7	using the determined signal delay to separate and define digital representations
8	of the in-phase DC offset voltage component and the quadrature phase DC offset voltage
9	component;
10	making the digital representation of each of the in-phase and quadrature phase
11	components more positive or more negative if it is more negative or more positive than a
12	predetermined minimum threshold or maximum threshold; and

a more positive or more negative value if the quadrature phase multiplication factor has a

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negative or positive value, respectively.

incrementally adjusting the signal value of the quadrature phase component to